

CLAIMS

1. A device comprising, between a differential pair of inputs, consisting of a first input (INN) and a second input (INP), and an output (OUT), a  
5 differential pre-amplifier (HPA1, HPA2), **characterised in that** said device further comprises an offset-reducing block (ORB) cascaded with said differential pre-amplifier (HPA1, HPA2) and arranged for reducing the offset generated by said differential pre-amplifier, and  
10 **in that** said device further comprises a buffering block (BB) in series with said offset-reducing block (ORB) and arranged for amplifying and buffering the output voltage of said offset-reducing block.

2. The device as in claim 1, **characterised in that** said differential pre-amplifier comprises a first (HPA1) and a second (HPA2) half pre-amplifier, each of said half pre-amplifiers having a first (+) and a second (-) input and an output, the outputs of said half pre-amplifiers being coupled together to form an input to said  
20 offset-reducing block (ORB).

3. The device as in claim 1 or 2, **characterised in that** the first input (+) of said first half pre-amplifier (HPA1) is coupled to a first input (INP) of said device, whilst the second input (-) of said  
25 first half pre-amplifier (HPA1) is coupled to the second input (INN) of said device, and  
**in that** the first input (+) of said second half pre-amplifier (HPA2) is coupled to the first input (INP) of said device, whilst the second input (-) of said second  
30 half pre-amplifier (HPA2) is coupled to the second input (INN) of said device.

4. The device as in any of the previous claims, characterised in that said offset-reducing block (ORB) comprises a transimpedance circuit.

5. The device as in claim 4, characterised  
5 in that said transimpedance circuit comprises a resistor (RP1) and an inverter stage (MP5-MN5).

6. The device as in any of the previous claims, characterised in that said offset-reducing block (ORB) additionally comprises means for equalisation.

10 7. The device as in claim 6, characterised  
in that said means for equalisation comprises a RC network.

8. The device as in any of the previous claims, characterised in that said buffering block (BB)  
15 comprises means for amplification and pulse shaping.

9. The device as in claim 8, characterised  
in that said means for amplification and pulse shaping comprises an inverter circuit (MN6-MP6).

10. A receiver structure comprising a device  
20 as in any of the previous claims.